Paper No. 20

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte ANTOINE DELARUELLE and FRANCISCUS A.M. VAN DE LAAR

Appeal No. 1999-2050
Application No. 08/576,544

ON BRIEF

Before BARRETT, FLEMING, and BARRY, Administrative Patent Judges.

BARRY, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the rejection of claims 1-9. We affirm-in-part.

BACKGROUND

The invention at issue in this appeal relates to memory access during convolutional interleaving and deinterleaving of data bits or symbols. Specifically, during the activation of a memory select line, data are both written to and read from

memory locations coupled to (i.e., selected by) the select line.

More specifically, a row select line is activated and a first column select line is activated to write data b(1,1,1) to a first memory location. A second column selection line is activated while the one row select line remains activated, and data b(1,1,1)@15 are read from a second memory location. Next, both the row select line and the second column select line remain activated and data b(1,2,1) are written into the second memory location. The activation of a subsequent column select line while the one row select line remains active and the reading and then writing of data to the selected memory locations continues for each cluster in the selected row.

The invention allows reading or writing in each clock cycle using a dynamic random access memory (DRAM). In addition, the continuous cycling through the DRAM allows memory refreshing cycles to be eliminated. Accordingly, clock frequency requirements are reduced resulting in reduced power requirements.

Claim 1, which is representative for our purposes, follows:

> 1. A method of interleaving a digital signal in which samples are delayed by an integral number times a unit delay, in accordance with a cyclically repeated delay pattern, comprising the following steps:
>
> cyclically activating parallel-arranged select lines of a memory at a cycle rate which is equal to the unit delay;
>
> writing to the memory, during one activation of a select line, a relevant bit of each sample to be delayed in an integral number of sample groups, a sample group being associated with one delay pattern cycle; and
>
> reading from the memory, during the one activation of the select line, which data includes a number of bits equal to the number of bits which is written, the bits being read in accordance with the delay pattern.

The reference relied on in rejecting the claims follows:

Ben-Efraim et al. (Ben-Efraim)	5,592,492	Jan. 7, 1997 (filed May 13, 1994).

Claims 1-7 and 9 stand rejected under 35 U.S.C. § 102(e) as anticipated by Ben-Efraim. Claim 8 stands rejected under 35 U.S.C. § 112, ¶ 2, as indefinite. Rather than repeat the

arguments of the appellants or examiner in toto, we refer the reader to the briefs and answer for the respective details thereof.

OPINION

In deciding this appeal, we considered the subject matter on appeal and the rejection advanced by the examiner. Furthermore, we duly considered the arguments and evidence of the appellants and examiner. After considering the record, we are persuaded that the examiner did not err in rejecting claims 1-5, 7, and 9. We are also persuaded that he did err in rejecting claims 6 and 8. Accordingly, we affirm-in-part. Our opinion addresses the anticipation and indefiniteness rejections.

Anticipation Rejection of Claims 1-7 and 9

When the appeal brief was filed, 37 C.F.R. § 1.192(c)(7) (1997) included the following provisions.

> For each ground of rejection which appellant contests and which applies to a group of two or more claims, the Board shall select a single claim from the group and shall decide the appeal as to the ground of rejection on the basis of that claim alone

> unless a statement is included that the claims of the group do not stand or fall together and ... appellant explains why the claims of the group are believed to be separately patentable. Merely pointing out differences in what the claims cover is not an argument ... why the claims are separately patentable.

In general, claims that are not argued separately stand or fall together. In re Kaslow, 707 F.2d 1366, 1376, 217 USPQ 1089, 1096 (Fed. Cir. 1983). When the patentability of dependent claims in particular is not argued separately, the claims stand or fall with the claims from which they depend. In re King, 801 F.2d 1324, 1325, 231 USPQ 136, 137 (Fed. Cir. 1986); In re Sernaker, 702 F.2d 989, 991, 217 USPQ 1, 3 (Fed. Cir. 1983).

Here, the appellant states, "[i]ndependent claims 1-5 ... are allowable or fall together." (Appeal Br. at 3.) Therefore, these claims stand or fall together as a group. We select
claim 1 to represent the group.

We note the following principles from Rowe v. Dror, 112 F.3d 473, 478, 42 USPQ2d 1550, 1553 (Fed. Cir. 1997).

> A prior art reference anticipates a claim only if the reference discloses, either expressly or inherently, every limitation of the claim. See Verdegaal Bros., Inc. v. Union Oil Co., 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "[A]bsence from the reference of any claimed element negates anticipation." Kloster Speedsteel AB v. Crucible, Inc., 793 F.2d 1565, 1571, 230 USPQ 81, 84 (Fed. Cir. 1986).

With this representation and these principles in mind, we address the appellants' arguments.

Regarding claims 1-5, the appellants argue, "the Examiner does not point out anywhere in the citation where means for 'activating parallel-arranged select lines of a memory' (as in each of the independent claims) is described ...." (Reply Br. at 2.) "In the patentability context, claims are to be given their broadest reasonable interpretations. Moreover, limitations are not to be read into the claims from the specification." In re Van Geuns, 988 F.2d 1181, 1184, 26 USPQ2d 1057, 1059 (Fed. Cir. 1993)(citing In re Zletz, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989)). Here, representative claim 1 specifies in pertinent part the following limitations: "activating parallel-arranged select lines of a memory ...." Giving the claim its broadest

reasonable interpretation, the limitations recite activating a memory's select lines, which are arranged in parallel.

Ben-Efraim teaches the limitations. The reference discloses a memory as "a plurality of shift register segments **34**, **36**, **38** and **40** having different lengths." Col. 3, ll. 9-11. Select lines are associated with each segment; the lines are arranged in parallel. Specifically, Ben-Efraim shows a line extending from the right side and another line extending from the left side of each segment. Fig. 2. The lines are shown as being in parallel. Furthermore, the lines are activated to select each segment. Specifically, "[t]he interleaver **30** is operated by using the switches **52** and **54** to sequentially select the segments **34**, **36**, **38** and **40**." Col. 3, ll. 27-29 (emphasis added).

Accordingly, we are persuaded that Ben-Efraim discloses the limitations of "activating parallel-arranged select lines of a memory ...." Therefore, we affirm the rejection of claims 1-5 as anticipated by Ben-Efraim.

Regarding claim 6, the appellants argue, "Ben-Efraim does not disclose 'data is both written to and read from memory during consecutive select line activations,' ...." (Appeal Br. at 5.) Claim 6 specifies in pertinent part the following limitations: "data is both written to and read from the memory during consecutive select line activations ...." Giving the claim its broadest reasonable interpretation, the limitations recite writing data to and reading data from the memory during consecutive select line activations.

The examiner fails to show a teaching of the limitations in Ben-Efraim. To the contrary, he admits, "when the switch 52 activates one of the segments to write a data to one of the shift register, the switch pointer 54 will activate the same segment to read the same data which written into the shift register." (Examiner's Answer at 7.) For its part, the reference teaches that "[a]fter a segment **34**, **36**, **38** or **40** is selected, the oldest symbol or data bit in the segment is read out from the right end of the respective shift register, a new symbol is written into the left end of the shift register, and

all other symbols are shifted to the right." Col. 3, ll. 36-40.

Because Ben-Efraim teaches writing data to and reading data from a shift register segment during the same select line activations, we are not persuaded that the reference discloses the limitations that "data is both written to and read from the memory during consecutive select line activations ...." Therefore, we reverse the rejection of claim 6 as anticipated by Ben-Efraim.

Regarding claim 7, the appellants argue, "Ben-Efraim does not disclose 'data is both written to and read from memory during all select line activations ... for each repeated delay portion,' ...." (Appeal Br. at 6.) Claim 7 specifies in pertinent part the following limitations: "data is both written to and read from memory during all select line activations ... for each repeated delay portion." Giving the claim its broadest reasonable interpretation, the limitations recite writing data to and reading data from the memory during the same select line activation.

Ben-Efraim teaches the limitations. Because Ben-Efraim teaches writing to and reading data from a shift register segment during the same select line activations, as mentioned regarding claim 6, we are persuaded that the reference discloses the limitations that "data is both written to and read from memory during all select line activations ... for each repeated delay portion." Therefore, we affirm the rejection of claim 7 as anticipated by Ben-Efraim.

Regarding claim 9, the appellants argue, "Ben-Efraim does not disclose 'reading to and writing from memory shifts ... the memory locations of interleaved bit groups,' ...." (Appeal Br. at 6.) Claim 9 specifies in pertinent part the following limitations: "the reading to and writing from memory shifts the data through the memory locations of interleaved bit groups." Giving the claim its broadest reasonable interpretation, the limitations recite that the reading data to and writing data from memory shifts the data through the memory locations.

Ben-Efraim teaches the limitations. Specifically, the reference discloses that "[a]fter a segment **34**, **36**, **38** or **40** is selected, the oldest symbol or data bit in the segment is read out from the right end of the respective shift register, a new symbol is written into the left end of the shift register, and all other symbols are shifted to the right." Col. 3, ll. 36-40 (emphasis added).

Accordingly, we are persuaded that Ben-Efraim discloses the limitations that "the reading to and writing from memory shifts the data through the memory locations of interleaved bit groups." Therefore, we affirm the rejection of claims 9 as anticipated by Ben-Efraim. Next, we address the indefiniteness rejection.

Indefiniteness Rejection of Claim 8

We note the following principles. “The test for definiteness is whether one skilled in the art would understand the bounds of the claim when read in light of the specification. If the claim read in light of the specification reasonably apprise[s] those skilled in the art

of the scope of the invention, Section 112 demands no more."

Miles Labs., Inc. v.

Shandon Inc., 997 F.2d 870, 875, 27 USPQ2d 1123, 1126 (Fed. Cir. 1993) (internal citations omitted). Furthermore, a claim should not be denied "solely because of the type of language used to define the subject matter for which patent protection is sought." In re Swinehart, 439 F.2d 210, 212 n.4, 169 USPQ 226, 228 n.4 (CCPA 1971). With these principles in mind, we consider the appellants' argument.

The appellants argue, "Figure 6a shows bit b(1,1,1.)@15 read from a memory location and figure 6b shows bit b(1,2,1) written to the same memory location. This is described in the specification at page 9, lines 19-31." (Appeal Br. at 4.) The examiner "still contends that the claimed subject matter that the 'data is both read and written to same memory in claim 8,' as claimed it reads as if the same data is read in the same memory not as appellant's argument that the data read and written being different data as described in the specification and shown in figures 6a and b." (Examiner's Answer at 4.)

Claim 8 specifies in pertinent part the following limitations: "the data is read and written into the same memory location in one cycle." The examiner fails to show that the limitations are indefinite. "Even if ... claims are .. broader than they otherwise would be, breadth is not to be equated with indefiniteness, as we have said many times." In re Miller,
441 F.2d 689, 693, 169 USPQ 597, 600 (CCPA 1971).

Here, although the relationship between the claimed electrically conducting storage and the claims contact opening may not be recited in claims 13-40, 53-60, 66, and 67, the omission is a matter of breadth, not of indefiniteness. Figure 6a of the specification shows that bit b(1,1,1.)@15 is read from a memory location; Figure 6b shows that bit b(1,2,1) is written to the same memory location. When read in light of the specification, one skilled in the art would understand that data are read from and written into the same memory location in one cycle. We demand no more. Therefore, we reverse the rejection of claim 8 as indefinite.

We end by noting that our affirmances are based only on the arguments made in the briefs. Arguments not made therein are not before us, are not at issue, and are considered waived.

CONCLUSION

In summary, the rejection of claims 1-5, 7, and 9 under 35 U.S.C. § 102(e) is affirmed. The rejection of claim 6 under § 102(e) and the rejection of claim 8 under 35 U.S.C. § 112, ¶ 2, are reversed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED-IN-PART

LEE E. BARRETT)
Administrative Patent Judge)
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